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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,556	03/29/2001	Terry L. Kendall	42390P10073	5873

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EXAMINER	
CONNOLLY, MARK A	
ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 10/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,556	KENDALL, TERRY L.	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-14,17-25,29,30,37 and 44* is/are rejected.

7)☒ Claim(s) *5,6,15,16,26-28,31-36,38-43 and 45-50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-50 have been presented for examination.

2. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 and 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al [James] US Pat No 6647512.

5. Referring to claim 1, James teaches the invention substantially including:

a. a first register to store default configuration data [col. 1 lines 17-20 and col. 6 lines 35-38].

b. a second register coupled to the first register to store active configuration data [col. 5 lines 18-22]. The system configuration parameters stored in CMOS are interpreted as active configuration data.

c. an input circuit coupled to the second register to receive input data different than the default configuration data to be programmed into the second register [col. 5 lines 23-31]. James explicitly teaches a user having the ability to change the system configuration parameters in the CMOS and it is obvious that there exists some circuitry to receive the

users input for those parameter changes. This obvious circuitry is interpreted as an input circuit. Furthermore, James explicitly teaches that the default CMOS configuration is loaded when the changes made by the user are incorrect which suggests that there is no correlation between the default configuration and the user configuration changes received by the input circuit.

Although James does not explicitly teach a control logic coupled to the first register, the second register and the input circuit to load the second register with data selected from either the default configuration data from the first register or input data from the input circuit, it is obvious that there needs to exist logic to control which data is to be written to the second register.

6. Referring to claim 2, James teaches a reset logic to select between loading the second register with the default configuration data and retaining a previous content of the second register in the second register [Abstract and col. 6 lines 35-38]. Unless the default configuration parameters are loaded into the CMOS, the previous configuration parameters will be retained in the CMOS.

7. Referring to claim 3, the "pressing and holding of the power button for 4 seconds while the computer is in a POST state ... to automatically restore backup settings to CMOS" as taught by James is interpreted as generating a reset signal to load default configuration data into the second register [col. 6 lines 35-39]. It is further interpreted that the signal is transmitted through a reset line.

8. Referring to claim 4, the reset line above is interpreted as a power-up reset line since the reset signal is generated during a POST state which occurs during power-up [col. 6 lines 35-39].

9. Referring to claim 7, it is interpreted by the examiner that the configuration parameters generated within the setup program are initially generated and temporarily stored apart from the second register until it is time for the second registers configuration parameters to be overwritten. It is further interpreted by the examiner that the newly generated configuration parameters are sent to the input circuit through a data bus so that the input circuit can then write the new parameter values into the second register.

10. Referring to claim 8, James teaches that the first register is a non-volatile register [col. 1 lines 17-20].

11. Referring to claim 9, James teaches that the second register is a volatile memory [col. 1 lines 33-40]. Volatile memories cannot retain their contents without power and James teaches that the CMOS is coupled to a battery to preserve its contents.

12. Referring to claim 10, James teaches that the first and second configurations are different because the contents of the CMOS are altered when the default configuration parameters are loaded into the CMOS [col. 5 lines 31-37 and col. 5 line 55 – col. 6 line 5].

13. Referring to claims 21-25 and 29, these are rejected on the same basis as set forth hereinabove. James teaches the apparatus and therefore teaches the method performed by the apparatus.

14. Referring to claim 30, it is obvious in the James system that the second register would be written to when a write-enable signal is asserted. Furthermore, the second register can only be written to from either the first register or the input circuit. Because the default configuration from the first register is written to when the reset signal is asserted, it is obvious that when the

reset signal is not asserted than the contents from the input circuit would be written to the second register.

15. Referring to claim 37, this is rejected on the same basis as set forth hereinabove. James teaches the apparatus and therefore teaches the system and method performed by the apparatus.

16. Claims 11-14 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over James as applied to claims 1-10 and 21-29 above, and further in view of Schmidt et al [Schmidt] US Pat No 6038689.

17. Referring to claim 11, this is rejected on the same basis as set forth hereinabove with the exception that James does not explicitly teach that the first and second registers, input circuit and control logic are included in a flash memory. Rather James teaches that the first and second registers are apart from each other in that the second register is a CMOS and the first register is some non-volatile memory. There is no suggestion that the two exist within a flash memory.

Schmidt explicitly teaches that a CMOS memory can be replaced with a flash memory [col. 3 lines 30-35]. It would have been obvious to one of ordinary skill in the art at the time of the invention to first, replace the CMOS memory taught in James with a flash memory because a flash memory does not require the use of a battery in order to preserve it contents thus eliminating the need for the CMOS battery which would free up extra space in the system. In addition, power consumption of the system would be reduced by not having to consume battery power while the system is powered off in order to preserve the configuration parameters. Secondly, it would have been obvious to include the first register in the flash memory since the first register is non-volatile and also to include the input circuit and control logic in the flash

memory as well. Since all these components work closely together as one system in order to input, save and restore configuration data, by integrating all these components into a single flash memory, the number of separate components could be reduced thus reducing the cost, size and complexity of the James-Schmidt system.

18. Referring to claims 12-20 and 44, these are rejected on the same basis as set forth hereinabove.

Allowable Subject Matter

19. Claims 5-6, 15-16, 26-28, 31-36, 38-43 and 45-50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
October 7, 2004